Improved breakdown voltage and impact ionization in InAlAs/InGaAs metamorphic high-electron-mobility transistor with a liquid phase oxidized InGaAs gate

Kuan-Wei Lee, Nan-Ying Yang, Mau-Phon Houng, and Yeong-Her Wang
Institute of Microelectronics, Department of Electrical Engineering, National Cheng-Kung University, Tainan 701, Taiwan

Po-Wen Sze
Department of Electrical Engineering, Kao-Yuan University of Technology, Lu-Chu, Kaohsiung 821, Taiwan

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The In$_{0.52}$Al$_{0.48}$As/In$_{0.53}$Ga$_{0.47}$As metal-oxide-semiconductor metamorphic high-electron-mobility transistors (MOS-MHEMTs) with a thin InGaAs native oxide layer (~10–15 nm) are demonstrated. The gate dielectric is directly obtained by oxidizing InGaAs material in a liquid phase solution. As compared to its counterpart MHEMTs, the MOS-MHEMTs have larger gate swing voltages, higher gate-to-drain breakdown voltages, and lower gate leakage currents with the suppressed impact ionization effect due to its higher barrier height. © 2005 American Institute of Physics.

The InAlAs/InGaAs metamorphic high-electron-mobility transistors (MHEMTs) on GaAs substrates have the characteristics of high gains and low noises in millimeter-wave applications and provide promising advantages over the structures grown on InP substrates such as being less expensive, less fragile, and available on a large scale. Many efforts have been made on the improvement of breakdown voltage and instability. To solve the first problem, a composite channel or doped channel has been used to overcome the small band-gap energy of the InGaAs channel. Besides, a higher aluminum content in the InAlAs Schottky layer also induces a gate leakage issue, which causes deterioration in device performances, especially when operating at high bias conditions. For the second problem, InP (Ref. 3) or InGaP (Ref. 4) has been used to reach long-term reliability and to act as an etching-stop layer in a selective-etch recessed-gate process. However, if the InP is used as a Schottky layer, a special structure must be involved to enhance the Schottky barrier height on InP (~0.5 eV), which may still suffer from the high gate leakage issue. Furthermore, insulators are the common choices on III-V compound semiconductors to increase the barrier potential with metal-oxide-semiconductor (MOS) gates to overcome the issues of maximum gate voltages, breakdown voltages, and gate leakage currents, which may limit the device applications. However, there is still the lack of a reliable low-temperature oxide film on InGaAs; moreover, there are very few reports that discuss InAlAs/InGaAs metal-oxide-semiconductor metamorphic high-electron-mobility transistors (MOS-MHEMTs). The MOS-MHEMT not only has the advantages of the MOS structure but also has the high-mobility two-dimensional electron gas (2DEG).

On the other hand, a variety of techniques such as plasma oxidation, a Si interfacial control layer, and Ga$_2$O$_3$(Ge$_2$O$_3$) have been used to passivate the InGaAs surface to form the metal-insulator-schottky-structure for better gate characteristics. However, these methods require very expensive systems, which complicate the fabrication processes. Furthermore, the deposition temperature is still high (>240 °C). In this letter, an alternative approach, liquid phase oxidation, is used to form the oxide (passivation) as the InGaAs gate dielectrics in InAlAs/InGaAs MOS-MHEMT applications. This is a simple, low-temperature (30–70 °C) method for growing uniform and smooth native oxide films on GaAs, AlGaAs, InGaP, InGaAs, and InAlAs. In this low-temperature system, neither anodic equipment nor an assisting energy source is needed. In our previous study, some oxide film issues were addressed and MOS-HEMTs were proposed.

The details of the oxidation system were reported earlier in Refs. 9 and 10. The oxidation rate is 10–15 nm/h in the growth solution with an initial pH=5.0 at 50 °C without pH control. The oxide layer is mainly composed of Ga$_2$O$_3$, although arsenic oxide and indium oxide may still remain to some extent confirmed by x-ray photoelectron spectroscopy (XPS). The oxide film is thermally stable, and the interface trap density is around 10$^{11}$ cm$^{-2}$eV$^{-1}$. InAlAs/InGaAs MHEMT structures were grown by metalorganic chemical-vapor deposition (MOCVD) on a semi-insulating GaAs substrate. The schematic structure of the device is shown in Fig. 1. Hall measurement indicates that the electron mobility is 7000 cm$^2$/V s and the electron sheet density is 2 $\times$ 10$^{12}$ cm$^{-2}$ at room temperature. The device isolation was accomplished by mesa wet etching down to the buffer layer. Ohmic contacts of the Au–Ge–Ni metal were deposited by evaporation, and then patterned by lift-off processes, followed by thermal annealing at 300 °C for 30–60 s. The oxidation procedure was to immerse the wafers into the growth solution to generate the gate oxide. Finally, the gate electrode was formed by lift-off process with Au.

Figure 2 shows the measured current-voltage (I–V) characteristics and the dependence of transconductance (g$_m$) for MHEMT with and without an oxide layer. The maximum gate voltage is larger than that of a conventional Schottky gate due to its higher energy barrier at the gate interface, which can enhance the current driving capability. In addition,
the drain current remains almost constant above the threshold voltage ($V_{th}$) at high drain biases due to the improvement of the impact ionization effect using MOS structure with a higher barrier height, which will be justified later. From Fig. 2(b), the maximum $g_m$ is 216 mS/mm at drain-to-source voltage $V_{DS} = 3$ V and the gate voltage swing is about 1 V. For a thicker oxide of 15 nm, the $V_{th}$ shifts to −0.5 V. The reduced maximum $g_m$ for a thicker oxide is due to the consumption of the InAlAs layer, resulting in a reduction in the 2DEG density. For $V_{th}$ shifts to the right, the separation between the InAlAs-oxide interface and the InGaAs channel layer is decreased due to the unique properties of the liquid phase oxidation with the reaction of InAlAs, resulting in the increased impact of the gate bias on the control of $V_{th}$ that is very attractive for the enhancement-mode fabrication. However, a decrease in the saturation current accompanies the degradation in the maximum $g_m$ of 150 mS/mm due to the reduction of effective carriers. This drawback can be overcome by a suitable device structure, such as inserting a Si-planar doping layer to increase the carrier density.

The oxide film provides an improvement in the breakdown voltage on account of the gate leakage current of the MOS structure. This can be further supported by typical gate-to-drain $I-V$ characteristics of MHEMT with and without an oxide film, as shown in Fig. 3. The forward turn-on voltage ($V_{ON}$) and the reverse gate-to-drain breakdown voltage ($V_{GD}$) are defined as the voltage at which the gate current density reaches 1 mA/mm. For MOS-MHEMT with 15-nm oxide thickness, the $V_{ON}$ is obviously higher than that of MHEMT (0.5 V) and the corresponding $V_{GD}$ are −27.4 V and −7.6 V, respectively. The gate leakage current can be suppressed by more than three orders of magnitude with a native oxide between the Schottky layer and the gate metal. The smaller gate leakage current is owing to the MOS structure and the elimination of sidewall leakage path passivated simultaneously during oxidation. Even with the sidewall passivation, however, there are unwanted detrimental indium and indium oxide distribution within the oxide film, resulting in a slight leakage between the exposed channel and the gate metal at the edge of the mesa. Besides, mesa etching may also contribute the Schottky-like $I-V$ characteristics for a forward $V_{ON}$. Even though the electrons are easier to obtain, sufficient energy to tunnel the oxide layer with increasing gate-to-drain voltage $V_{GD}$ (toward positive values), especially in the thin oxide case; however, they must still have enough energy to surmount the high barrier potential due to the oxide layer and to enter the InAlAs layer with a decreasing $V_{GD}$.

In order to gain better insight on the influence of impact ionization that results in high drain conductance and $g_m$ compression, the gate current density as a function of gate-to-source voltage $V_{GS}$ is measured. The bell-shaped curve is the typical behavior of the impact ionization as shown in Fig. 4. At pinch off, the current from the tunneling effect is observed, which is very small due to the large
diode breakdown voltage for MOS-MHEMT; however, at the open channel, the impact ionization current is observed. Clearly, a remarkable increase in the gate current takes place when devices are biased at higher $V_{DS}$. Due to the existence of a high electric field in the gate-to-drain region, significant hot electron phenomena happen in the narrow band-gap InGaAs channel, i.e., electrons can obtain higher energy to generate electron-hole pairs through enhanced impact ionizations, resulting in easier injection of holes into the gate terminal. However, the peak gate current density for MOS-MHEMT is significantly improved as compared with that of MHEMT. In other words, the electrons and holes generated by the impact ionization are decreased to further reduce the drain and gate current owing to the liquid phase oxide layer with a high barrier height, which is consistent with the results of Figs. 2(a) and 3.

In summary, the oxidized InGaAs as the gate dielectric of InAlAs/InGaAs MOS-MHEMT prepared by the liquid phase oxidation near room temperature before gate metallization has been demonstrated. As compared to the conventional MHEMT, larger gate voltages, higher breakdown voltages, and lower gate leakage currents with the suppressed impact ionization effect for the MOS-MHEMT make the proposed simple and low-temperature liquid phase oxidation suitable for device applications.

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